Automatic Swing Control in Relaxation Oscillators

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Abstract—An automatic swing control (ASC) feedback is presented for relaxation voltage-controlled oscillators (VCO's). The ASC feedback maintains the oscillation swing at a constant level by dynamically adjusting the threshold voltage of the oscillator. The feedback mechanism provides a very wide linear frequency range and pushes saturation in the frequency characteristic of the oscillator to higher frequencies. As a result, operation close to the maximum achievable frequency, set by the inherent delay of the oscillation loop, becomes practically possible. Also, the sensitivity of the VCO frequency characteristic to process and temperature variations is reduced. These features make the ASC oscillator particularly suitable for autorate operation in serial–digital video applications. Detailed description of the design and experimental results of a trimmable VCO are given in this paper. It is shown that the frequency range is increased from 20–500 to 20–800 MHz when the ASC feedback is applied. In addition, statistical data from more than 1000 samples from several batches before and after trimming are provided. The results confirm the manufacturability of the ASC feedback approach. The implementations were done in a semicustom 14-GHz bipolar process.

Index Terms— Analog integrated circuits, bipolar transistor oscillators, oscillators, relaxation oscillators, voltage-controlled oscillators.

I. Introduction

THE operation of a relaxation oscillator is based on alternately charging and discharging a capacitor by a reference current [1]. Relaxation-based voltage-controlled[1] oscillators (VCO's) have been designed to operate up to several gigahertz [2]. Compared to ring and inductance–capacitance (LC)-tuned oscillators, they provide the widest tuning range and the best linear voltage-to-frequency characteristic. However, these oscillators usually suffer from poorer noise performance [3].

In a bipolar process, a relaxation oscillator can be realized as either an emitter- or a collector-coupled configuration [1], [4]. In the emitter-coupled configuration, sudden voltage jumps appear at both ends of the floating capacitor, where usually large parasitic capacitors to either substrate or ground are present. These jumps create excessive current spikes and possible substrate injection. On the other hand, the floating capacitor in a collector-coupled configuration does not experience sudden voltage jumps [4].

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[1] The controlling parameter is a current rather than a voltage, and usually a voltage-to-current converter is used.

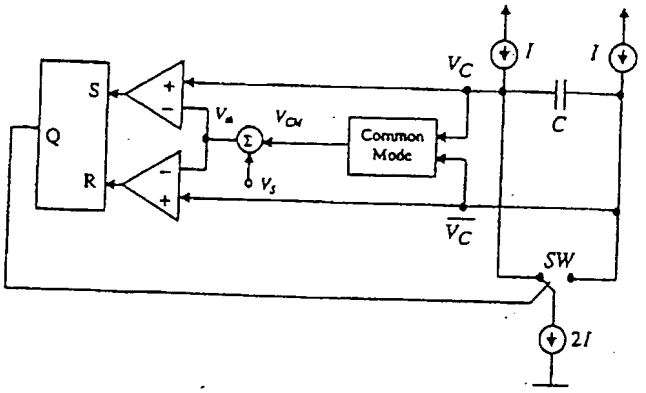

Fig. 1. A typical relaxation oscillator.

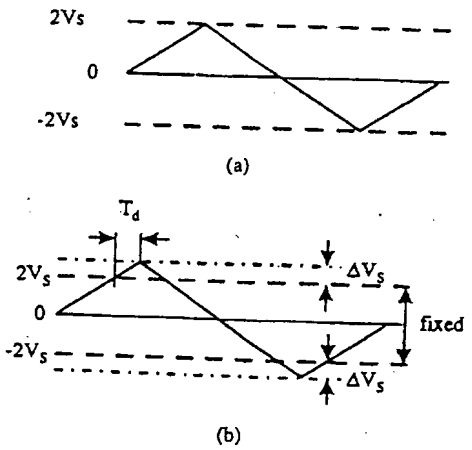

Fig. 2. Voltage waveform across the capacitor: (a) ideal case and (b) nonideal case.

Fig. 1 shows a simplified block diagram of a collector-coupled relaxation oscillator. For the switch position shown in this figure, the voltage at node $\overline{V}_C$ increases linearly until it reaches the threshold level V_{th}. At this time, the latch is reset and the polarity of the current through the capacitor is reversed. The capacitor voltage starts to increase in the opposite direction until V_C reaches the threshold level. This sets the latch and completes one cycle of oscillation. As a result, the voltage across the capacitor swings with a peak amplitude of $2V_S$, where $V_S = V_{th} - V_{CM}$ (V_{CM} is the common-mode voltage of V_C and $\overline{V}_C$). In practice, V_{CM} is set to a reference value in a common-mode feedback loop, not shown in Fig. 1 for simplicity. The capacitor voltage waveform is illustrated in Fig. 2(a). In the ideal case, the frequency of oscillation is linearly dependent on the current and inversely proportional to the capacitance and its voltage

swing

$$f = \frac{I}{8CV_S}. \tag{1}$$

To derive this formula, it is assumed that as soon as V_C or $\overline{V}_C$ reaches V_{th}, the switch toggles instantly. However, there is a delay associated with the comparator, the set–reset (SR) latch, and the switch. During this delay T_d, the voltage across the capacitor continues to rise or fall in the same direction by the amount $\Delta V_S = IT_d/C$, as shown in Fig. 2(b). As a result, the voltage swing across the capacitor is no longer fixed, and the actual amplitude of the capacitor voltage swing becomes

$$V_{S\_act}(I) = 2V_S + \frac{IT_d}{C}. \tag{2}$$

The above change in the capacitor swing can be viewed as an increase in the threshold voltage, making it a function of the charging current

$$V_{th\_act}(I) = V_{CM} + V_S + \frac{IT_d}{2C}. \tag{3}$$

As a result, the frequency of oscillation drops to

$$f = \frac{I}{4CV_{S\_act}} = \frac{1}{\frac{8CV_S}{I} + 4T_d}. \tag{4}$$

As (4) shows, the linear relationship between current and frequency is approximate. At low frequencies, T_d can be ignored and linearity is good. At high frequencies, T_d is comparable with the period of oscillations, and consequently, the I–F characteristic becomes nonlinear. Also, when I is increased, the frequency slowly approaches its maximum limit of

$$f_{\text{lim}} = \frac{1}{4T_d}. \tag{5}$$

However, operation of the oscillator close to f_{lim} is practically impossible because of the excessive current requirement. Furthermore, since the capacitor voltage swing increases with I, the circuit should be designed to handle a much larger voltage swing. As the delay T_d is dependent on temperature and process, the sensitivity of the oscillator to these factors increases as the frequency increases. For autorate operation in serial–digital video applications [5], where operation at multiple center frequencies is required, it is desired to design the VCO such that its voltage-to-frequency characteristic is insensitive to process and temperature variations over a wide frequency range. The presence of T_d in (4) indicates that this goal cannot be achieved by trimming the VCO at one frequency. In the following section, a feedback control over the oscillator threshold voltage will be introduced to overcome the aforementioned limitations.

II. The Automatic Swing Control Concept

The basic idea in ASC feedback is to replace the fixed swing voltage, V_S in Fig. 1, with a variable voltage [6]. This voltage is adaptively adjusted to compensate for the threshold increase described by (3). Fig. 3 shows the block diagram of a relaxation VCO that incorporates the ASC feedback loop. Here, the desired voltage swing of the capacitor is applied to the oscillator as the reference voltage of the control loop V_{ref}. The capacitor voltage swing is extracted by subtracting the average voltage of V_C and $\overline{V}_C$ from their peak value. The extracted swing is compared with the reference voltage to generate an error signal, which is then amplified and low-pass filtered. The resulting signal, when added to the common-mode voltage V_{CM}, provides the oscillator with a threshold level that could vary between V_{CM} and $V_{CM} + V_{\text{ref}}$. By having a large dc gain in the ASC feedback loop, the threshold voltage settles at a level that forces the error signal to almost zero. As shown in Fig. 4, the voltage swing across the capacitor becomes independent of the charging current and has a constant peak amplitude of $2V_{\text{ref}}$. The frequency becomes a linear function of the current even at high frequencies

$$f = \frac{I}{8CV_{\text{ref}}} \qquad \text{for } f < f_{\text{lim}} \tag{6}$$

where f_{lim} is set by the process and is given by (5). Furthermore, operation close to this frequency is achievable in practice because the feedback loop can force V_S to zero. Also, note that high-frequency operation of the ASC VCO does not require the excessive current that is predicted by (4) for a conventional relaxation VCO. Fig. 5 is a typical illustration of the frequency and voltage swing characteristics of the conventional and ASC relaxation VCO's shown in Figs. 1 and 3. Note that for the ASC oscillator, the swing is kept constant up to the point where the feedback loop has decreased V_S

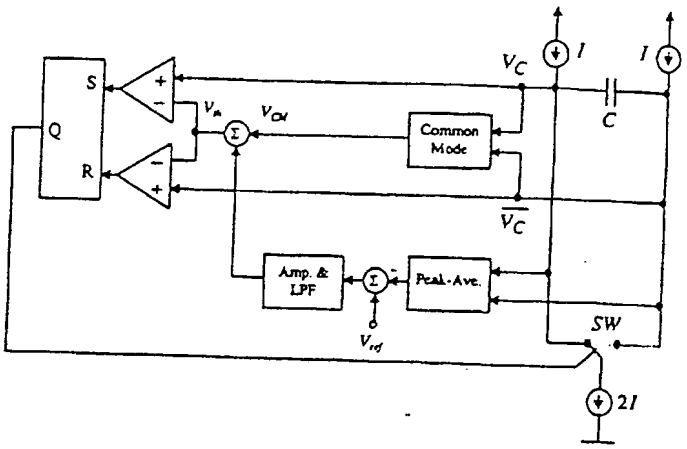

Fig. 3. ASC relaxation oscillator.

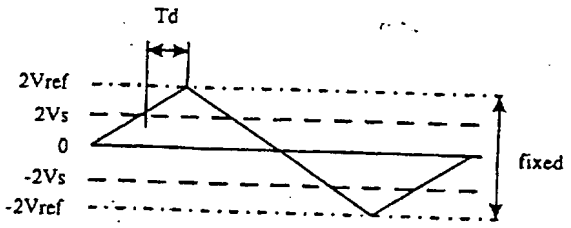

Fig. 4. Voltage waveform across the capacitor in the ASC VCO.

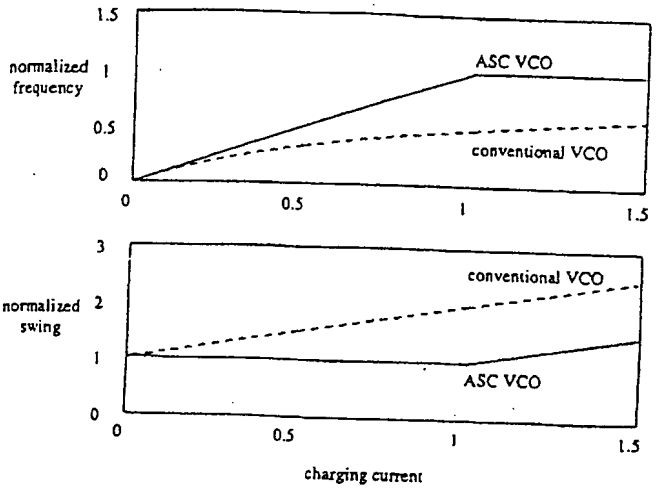

Fig. 5. Frequency and swing characteristics of the conventional and ASC relaxation VCO's (frequency is normalized to its maximum and swing to its minimum).

down to zero. At this point, the frequency has reached its limit and cannot be increased beyond that.

III. Circuit Description

A. Relaxation VCO

Fig. 6 shows the circuit diagram of the collector-coupled relaxation VCO. In accordance with Fig. 1, this circuit was designed and fabricated as our reference for evaluating the performance of the VCO after the ASC loop was added. Here, transistors Q_1 and Q_2 form the switch SW and direct current I_C to charge and discharge capacitor C_1. Pullup resistors R_1 and R_2 are used instead of current sources to eliminate the need for a common-mode feedback and PNP or PMOS transistors. The available PNP transistors in our process have a low early voltage, high parasitic capacitances, and low beta. To achieve a reasonable beta, many PNP transistors are required. This increases the parasitics to a value close to C_1. In addition, a beta-compensation circuit for PNP transistors is required to handle the wide variations in I_C. Q_3, Q_4, and R_3 in Fig. 6 act as a negative resistance to compensate for the current variations in the pullup resistors due to the voltage swing across them [7]. As a result, capacitor C_1 is charged and discharged with a constant current. It should be mentioned that in this approach, the common-mode voltage V_{CM} is a function of I_C. The variation in V_{CM} results in a change in the junction capacitors at nodes V_C and $\overline{V}_C$. However, these changes are small compared to C_1 and have a negligible effect on the frequency of oscillation. R_6, R_7, and C_2 extract the common-mode voltage of the capacitor terminals. This voltage is buffered by Q_9 and serves as the threshold voltage of the SR latch. The latch consists of Q_5, Q_6, R_4, and R_5. Assuming Q_5 is on and Q_6 is off, the voltage at the base of Q_7 is compared with that of Q_5, which is effectively the emitter voltage of Q_9. As soon as this voltage passes the threshold level, Q_7 starts to conduct and, through the positive feedback of the latch, turns off Q_5 and turns on Q_6. This changes the state of the latch, and consequently the state of the switch, and reverses the direction of the current through C_1.

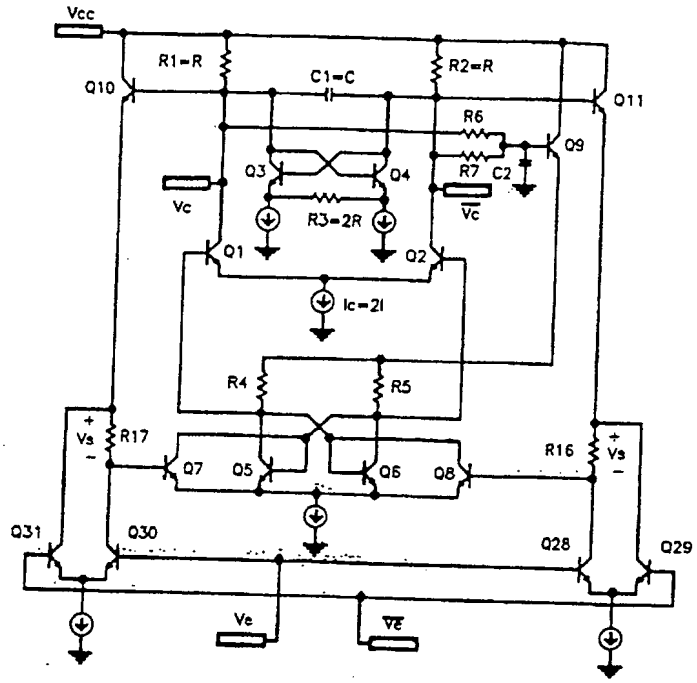

Fig. 6. Circuit diagram of the conventional relaxation oscillator.

The mechanism through which the swing amplitude is set is slightly different from (but equivalent to) what was shown in Fig. 1. Rather than being added to the common-mode voltage, the reference voltage is subtracted from both V_C and $\overline{V}_C$ through dc voltage drops across resistors R_{17} and R_{16}. Transistors Q_{10} and Q_{11} buffer V_C and $\overline{V}_C$ before level shifting. These transistors also compensate for the V_{BE} drop of Q_9, which is used to buffer V_{CM}. For best compensation, the currents of these three transistors should be equal. DC-level-shifted versions of V_C and $\overline{V}_C$ are fed to the bases of Q_7 and Q_8 to toggle the state of the latch.

The differential voltage applied to V_e and $\overline{V}_e$ controls the amount of the current through R_{16} and R_{17} by bypassing some of the bias currents of differential pairs Q_{28}–Q_{29} and Q_{30}–Q_{31}. However, to keep the currents of transistors Q_{10} and Q_{11} constant and independent of the amount of dc shift V_S, the bypassed currents are added to the currents of R_{16} and R_{17}. Although V_e and $\overline{V}_e$, and hence V_S, are constant for our conventional VCO, this will not be the case once the ASC feedback is established.

In our implementation, the charging current I_c consists of two components: a coarse-tuning current and a fine-tuning current. This is to achieve the multiple center frequency requirement. These components are both generated by applying an internal bandgap voltage to an external resistor. Therefore, I_c is almost independent of process, temperature, and supply-voltage variations.

B. Relaxation VCO with ASC

Fig. 7 shows the circuit diagram of the ASC feedback, which was designed to be added to the conventional VCO described above. In this circuit, transistors Q_{18} and Q_{19} and

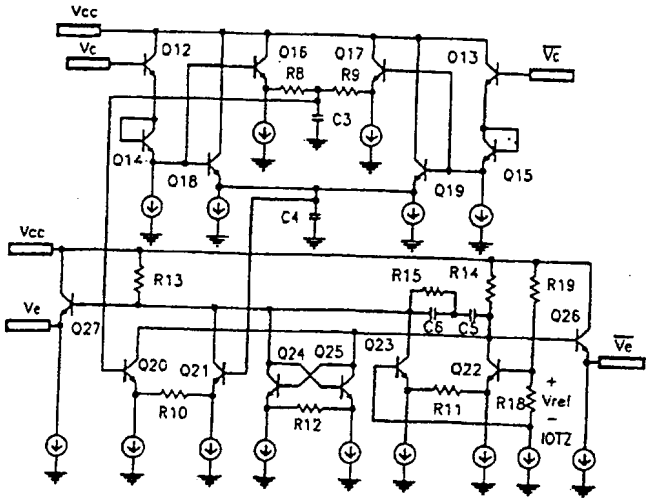

Fig. 7. Circuit diagram of the ASC feedback, which can be added to the oscillator of Fig. 4.

capacitor C_4 extract the peak voltage of shifted versions of V_C and $\overline{V}_C$. Q_{16}, Q_{17}, R_8, R_9, and C_3 extract the common-mode value of these voltages. The degenerated differential cell, consisting of Q_{20}, Q_{21}, and R_{10}, converts the difference between the peak and common-mode voltages into a differential current. This current, which is representative of the oscillator swing, is subtracted from a reference current. The reference current is generated by applying the reference voltage V_{ref} to a matched degenerated differential cell composed of Q_{22}, Q_{23}, and R_{11}. The net differential error current is converted back to voltage by resistors R_{13} and R_{14}. Q_{24}, Q_{25}, and R_{12} are configured in a positive feedback to enhance the voltage gain of the error amplifier. The value of R_{12} was chosen to be slightly more than the sum of R_{13} and R_{14} and matched to them. This guarantees that the positive feedback never causes a latchup. The low-pass filter composed of C_5, C_6, and R_{15} filters the error signal. This filter stabilizes the feedback loop and filters out the ripples introduced by the peak detector. When the ASC circuit is connected to the VCO of Fig. 6, the differential error signal $V_e - \overline{V}_e$ adjusts V_S, as explained earlier. It should be pointed out that this filter puts a constraint on the modulating frequency when the VCO is modulated by an external control voltage. For high modulating frequencies, the ASC loop fails to respond and the VCO gain drops to that of the conventional VCO. Therefore, the time constant of the ASC loop, set by the low-pass filter, must be chosen according to the maximum modulating frequency.

The reference voltage V_{ref} is used to compensate for temperature and process variations of the oscillator. In the present VCO, the frequency of oscillation tends to decrease with temperature due to parameters such as positive temperature coefficient of C_1, increase in the switching time of Q_1 and Q_2, and temperature response of our ASC feedback circuit. This temperature dependency can be compensated by decreasing V_{ref}. The process variations can also be canceled out by trimming this voltage. Therefore, V_{ref} should have an appropriate combination of the following components: a component that has a negative temperature coefficient, a component that can be trimmed, and a component with a fixed value. In our implementation, V_{ref} is generated by passing a current I_{OTZ} through the internal resistor R_{18} shown in Fig. 7. As shown in Fig. 8, the current I_{OTZ} is composed of three components. The first component I_O is generated by applying a bandgap voltage across an internal resistor. This part develops a fixed voltage drop across R_{18}, independent of process and temperature. The second component I_T is generated by a V_{BE} drop across an internal resistor and develops the voltage with the negative temperature coefficient. The third component I_Z, which can be trimmed with 6 bits of accuracy, generates a trimmed temperature-independent voltage. By on-wafer trimming of the current I_Z, the reference voltage V_{ref} is permanently adjusted such that a target frequency of oscillation is achieved at a predetermined amount of current I_c. The proper combination of I_O and I_T was first chosen based on simulations and was later adjusted based on measurement results. It should be pointed out that the ASC feedback removes the effect of T_d and consequently its large process-dependent effect on the oscillation frequency. Therefore, trimming at one frequency results in trimming the VCO from low frequencies (where T_d is negligible) up to high frequencies (where T_d is comparable to the period of oscillation).

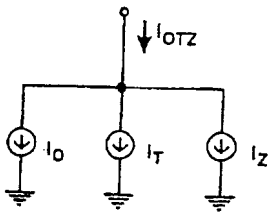

Fig. 8. Current I_{OTZ}.

IV. Simulation Results

In this section, some of the simulation results for the VCO are provided to further demonstrate the effectiveness of the proposed ASC feedback. We will first compare the performance of the oscillators with and without ASC. Next, we will show how the ASC oscillator performs over process variations. Last, we will demonstrate how trimming can compensate process variations in the ASC oscillator.

The relaxation oscillator was simulated both with and without the ASC feedback (Figs. 6 and 7). This VCO was intended to be used in a phase-locked loop with a maximum loop bandwidth of few megahertz. The bandwidth of the ASC feedback loop was chosen to be 10 MHz. Therefore, the modulating frequency of the VCO is well within the frequency response of the ASC. The frequency and the peak value of the signal swing of the capacitor versus current are shown in Fig. 9. As can be seen, by applying the ASC, the linear frequency range of the VCO is extended significantly. The I–F characteristic of the VCO without ASC starts to bend at about 200 MHz, while the I–F characteristic of the ASC VCO goes up to about 700 MHz before starting to bend. The ASC feedback is also seen to increase the frequency of oscillation at the current level of 7 mA from 625 to 950 MHz. This

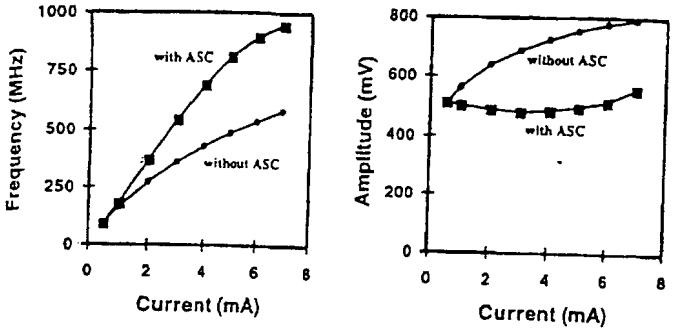

Fig. 9. Frequency and amplitude of oscillations with and without ASC.

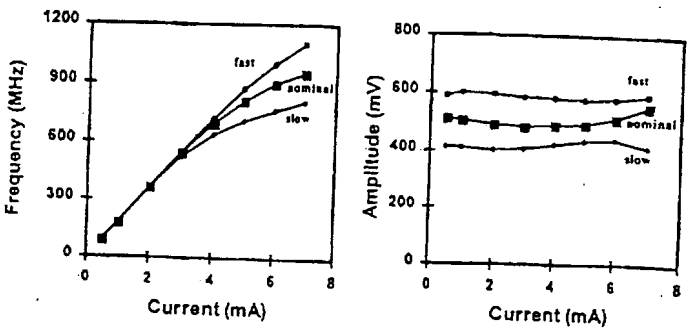

Fig. 11. Frequency and amplitude of oscillation of the ASC oscillator after trimming.

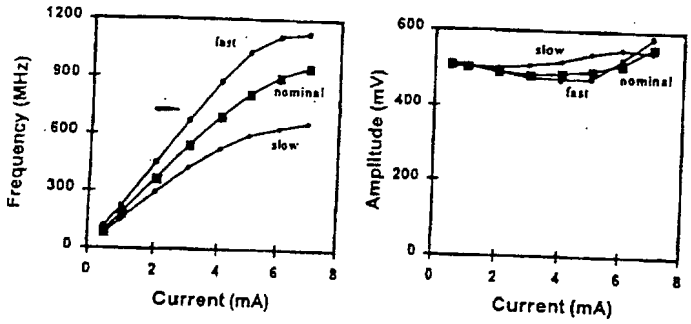

Fig. 10. Frequency and amplitude of oscillation of the ASC oscillator under process variation.

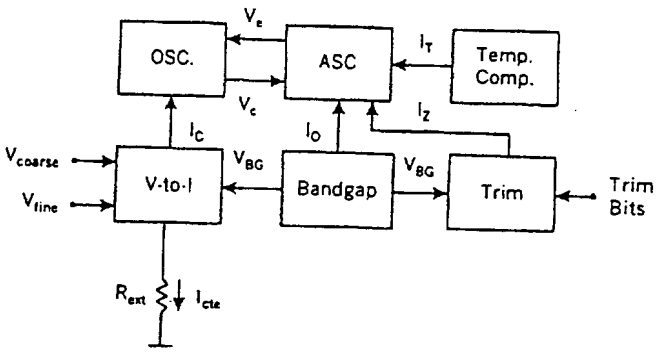

Fig. 12. Block diagram of the chip.

has been achieved by keeping the amplitude of oscillation fairly constant at about 500 mV (twice the reference voltage) and preventing it from increasing to 800 mV, as shown in Fig. 9.

Fig. 10 shows the characteristics of the ASC VCO simulated using the "nominal" model and two corner models "fast" and "slow," which cover the effect of process variations on the oscillator. In all three cases, the ASC feedback loop keeps the signal swing across the capacitor almost constant. However, because of different capacitance values in the three models (a variation of ±20%), the I–F curves have different slopes: the largest slope for the "fast" case and the smallest slope for the "slow" case. The maximum frequency depends on the delay that is the smallest in the "fast" case (where we see the highest frequency) and the largest in the "slow" case (where we see the lowest frequency).

To have a VCO with an I–F characteristic independent of process, the voltage V_{ref} is trimmed. As discussed in the previous section, V_{ref} is adjusted such that at a given current, the frequency of oscillation is that of the nominal process. In our simulation, the signal swing of the "fast" case must be increased to 600 mV, whereas the signal swing of the "slow" case must be decreased to 400 mV. Fig. 11 shows the simulation results of the ASC VCO after trimming at $I_c = 1$ mA, corresponding to a frequency of 180 MHz. The I–F characteristics overlap up to about 600 MHz. Above 600 MHz, the I–F characteristic for the slow" case starts to saturate toward its maximum value of 00 MHz. The frequency for the "fast" case overlaps the nominal" frequency up to about 800 MHz. It should be pointed out that trimming does not affect the maximum limit of the oscillation frequency, which is dictated by the delay T_d.

V. Implementation

The ASC VCO was designed to have a frequency sweep range of 20–800 MHz [8]. The circuit was fabricated on a semicustom array in a bipolar process that offers NPN transistors with a cutoff frequency of 14 GHz and lateral PNP transistors with a cutoff frequency of 50 MHz. This process has two metal layers, poly resistors, and MOS and metal-to-metal capacitors.

Fig. 12 shows the block diagram of the implemented chip. A bandgap voltage is applied to an external resistor to generate a constant current I_{cte}. The voltage-to-current converter, which has a coarse and a fine tune input, generates the charging current I_c from I_{cte}. With the right combination of V_{coarse} and V_{fine}, shown in Fig. 12, the center frequency and tuning range of the VCO are set. The circuit schematics of the oscillator core and ASC blocks were shown in Figs. 6 and 7 and were discussed in detail in previous sections. The ASC block receives the currents I_O, I_T, and I_Z from the bandgap, temperature compensation, and trim blocks, respectively. The trim block provides on-wafer trimming capability, which can be used to trim the center frequency of the VCO to within ±0.4%. Having six trim bits allows successful trimming of the devices that experience a process variation of up to 50%. The micrograph of the implemented chip is shown in Fig. 13 with the various blocks highlighted.

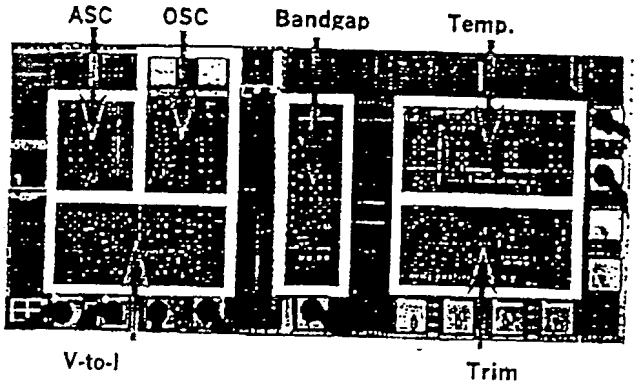

Fig. 13. Micrograph of the chip.

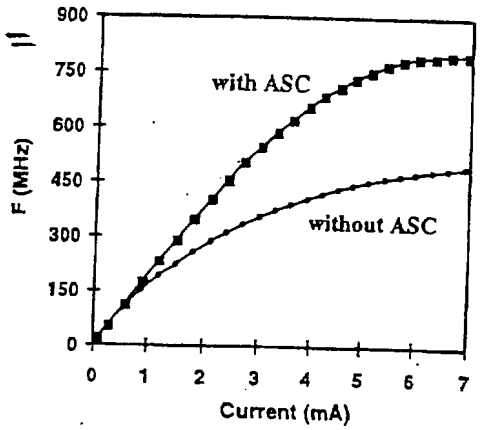

Fig. 14. Measured I–F characteristic of the oscillator.

VI. Experimental Results

Fig. 14 shows the measured I–F characteristic of the oscillator. With the ASC feedback inactive, the oscillator works up to only 500 MHz. A further increase in the current does not increase the frequency, as the voltage swing is also increased due to the effect of T_d. Once the ASC feedback is added, the frequency of oscillation reaches 800 MHz. Also, the linear range of the characteristic becomes considerably wider. These are in accordance with the theory and simulation results discussed earlier. It should be pointed out that as the current is reduced, the common-mode voltage of the capacitor terminals approaches the supply voltage and reduces the headroom for the capacitor voltage swing. This limits the low-frequency operation of the VCO to 20 MHz in both cases.

Fig. 15 shows the statistical data before and after trimming of more than 1000 IC's gathered from ten wafers fabricated in different process runs. As seen in Fig. 15(a), the frequency at a current of I_{c1} has a mean value of 351 MHz with a standard deviation of 87.4 MHz. Of these devices, only 5.5% experienced a process variation greater than 50% and were rejected. For the remaining 94.5%, on-wafer trimming was performed at the current level I_{c1}. The target frequency was 330 MHz, and the resulted standard deviation was 1.7 MHz. By switching the current to I_{c2}, the frequency had a mean value of 494.2 MHz and a standard deviation of only 3.7 MHz. The histograms after trimming are shown

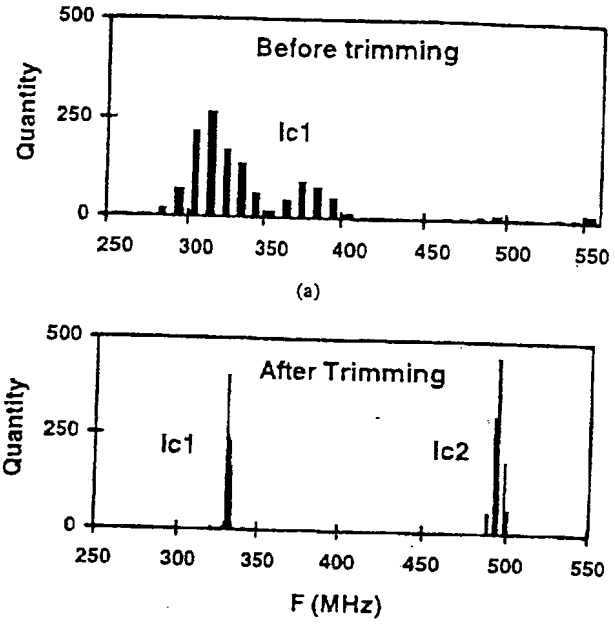

Fig. 15. Statistical data (a) before and (b) after trimming.

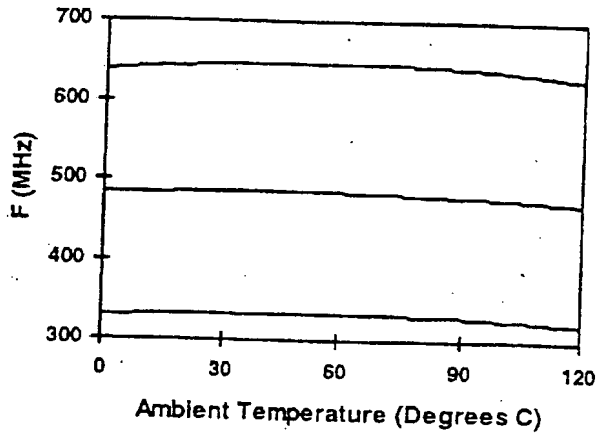

Fig. 16. Measured temperature behavior.

in Fig. 15(b). The small standard deviation at the second frequency is an indication that the I–F characteristics of the trimmed IC's overlap regardless of the process variation. Therefore, current switching can be used to achieve a relatively accurate frequency switching. The process independence of the I–F characteristic of the ASC VCO makes it attractive in autorate serial–digital video applications where a single VCO is required to operate in various frequency bands over a wide frequency range.

Fig. 16 illustrates the temperature measurements at three different operating frequencies of a plastic-packaged ASC VCO. A temperature coefficient better than -230 ppm/°C is achieved over a span of 120°C. It should be mentioned that as temperature rises, T_d increases and, consequently, f_{lim} drops. However, for frequencies below f_{lim}, the ASC feedback removes the effect of T_d and allows the temperature-compensation circuit to be effective even at an ambient temperature as high as 120°C. The plastic-packaged part was also

TABLE I
TEMPERATURE MEASUREMENTS UNDER SUPPLY VARIATIONS

Supply Voltage (V)		Ambient Temperature (Degrees C)						
		0	20	40	60	80	100	120
4.75	F1 (MHz)	331	332	333	332	331	327	321
	F2 (MHz)	486	487	487	486	484	480	474
	F3 (MHz)	637	644	646	646	644	639	630
5.00	F1 (MHz)	330	332	332	332	331	327	321
	F2 (MHz)	484	485	486	485	482	478	472
	F3 (MHz)	637	644	646	646	644	638	628
5.25	F1 (MHz)	330	332	332	332	330	327	320
	F2 (MHz)	483	484	485	483	481	477	469
	F3 (MHz)	637	644	646	646	643	637	626

TABLE II
POWER-SUPPLY REJECTION MEASUREMENTS

f_n (MHz)	100	200	300	400	500	600
PSRR at f_n (dB)	44	53	40	50	33	36
PSRR at f_n offset from carrier (dB)	32	30	30	34	26	32

TABLE III
PERFORMANCE SUMMARY

Supply Voltage	5V
Supply Current	18mA
Frequency Range	20-800MHz
Tuning Range	30% of center frequency
Phase Noise (370MHz)	-99dBc/Hz@2MHz offset
PSRR	>26dB
Temperature Coefficient	-230ppm/°C over 120°C
Trim Accuracy	± 0.4% of center frequency
Trim Range	50% of center frequency
Technology	14GHz-f_T bipolar, semi-custom

tested over supply variations of ±5% across the 0–120°C temperature range. The results are summarized in Table I. For the stated change in the supply voltage, the frequency changes by only 0.6% at room temperature and changes not more than 1% over the entire temperature range.

The chip operates from a nominal power supply of 5 V and draws a total current of 18 mA.[2] The tuning range of the VCO is 30% of its center frequency. The phase noise of the oscillator measured at 370 MHz is −99 dBc/Hz at 2-MHz offset. To measure the power-supply rejection, a 100-mV_{rms} sinusoidal waveform was added to the supply voltage. This generates dominant tones at the applied frequency f_n and its folded frequency around the carrier. The power-supply rejection ratio (PSRR) at various applied frequencies is given in Table II. In this test, the carrier frequency was set to 580 MHz and had an output power of −4.3 dBm. A rejection of better than almost 30 dB was observed. Table III summarizes the performance of the chip.

VII. CONCLUSIONS

An ASC was presented for use with relaxation oscillators. It was shown that ASC both increases the linear frequency range and reduces the sensitivity of the oscillator to process and temperature variations. A collector-coupled relaxation oscillator was implemented in a 14-GHz bipolar process. While with ASC the frequency reaches 800 MHz, without ASC it goes up to only 500 MHz. Statistical data were presented showing that by trimming the ASC VCO, the I–F characteristic becomes independent of process variations over a wide frequency range. This means that only one external resistor and a V–I converter are required to adjust the frequency in various bands over a wide range. These features make the ASC VCO attractive in autorate serial–digital video applications.

[2]A full-custom approach reduces the parasitic capacitances and requires less driving currents. As a result, the higher limit of the operating frequency can be achieved with a smaller supply current.

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